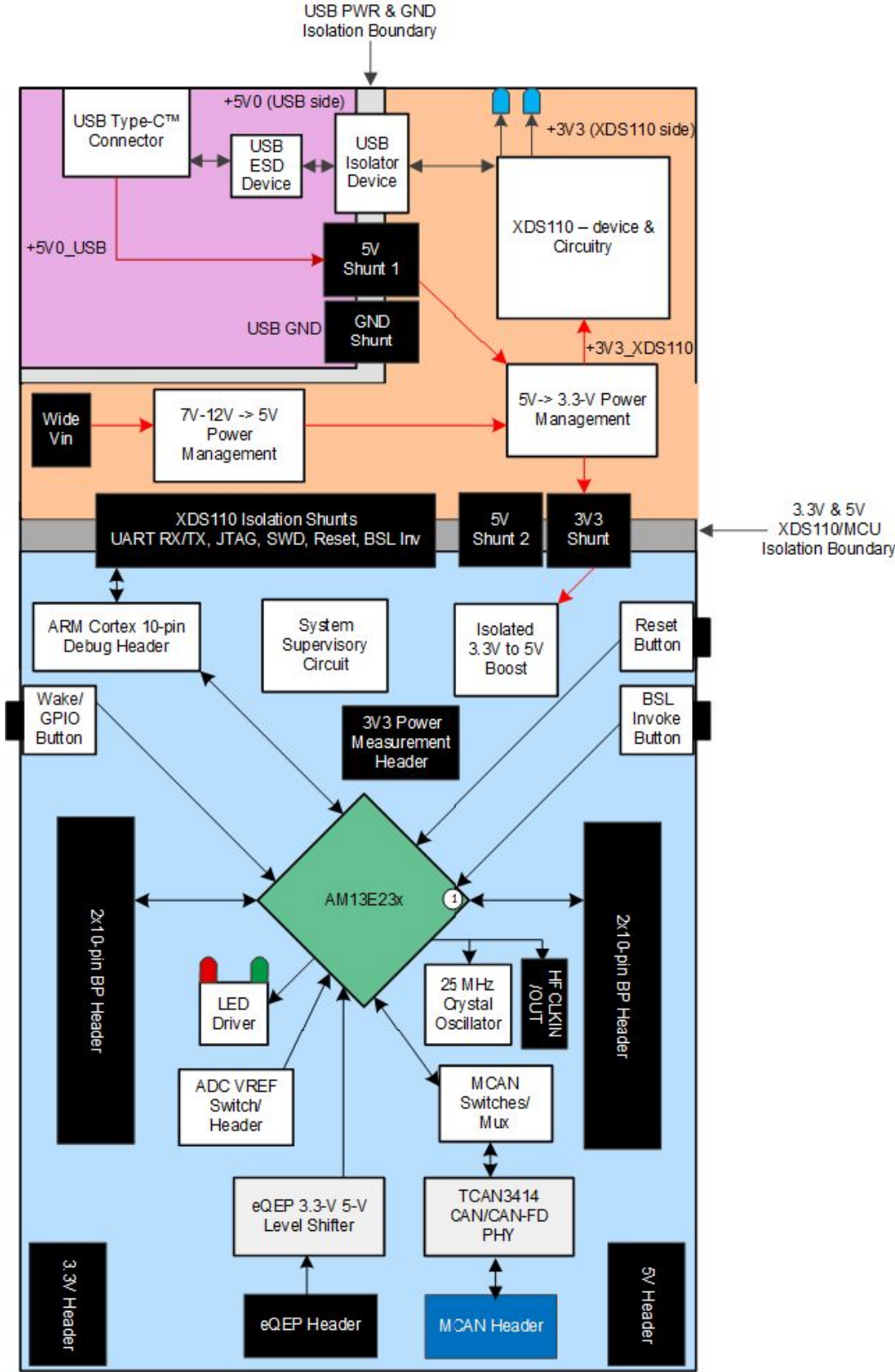


LP-AM13E230

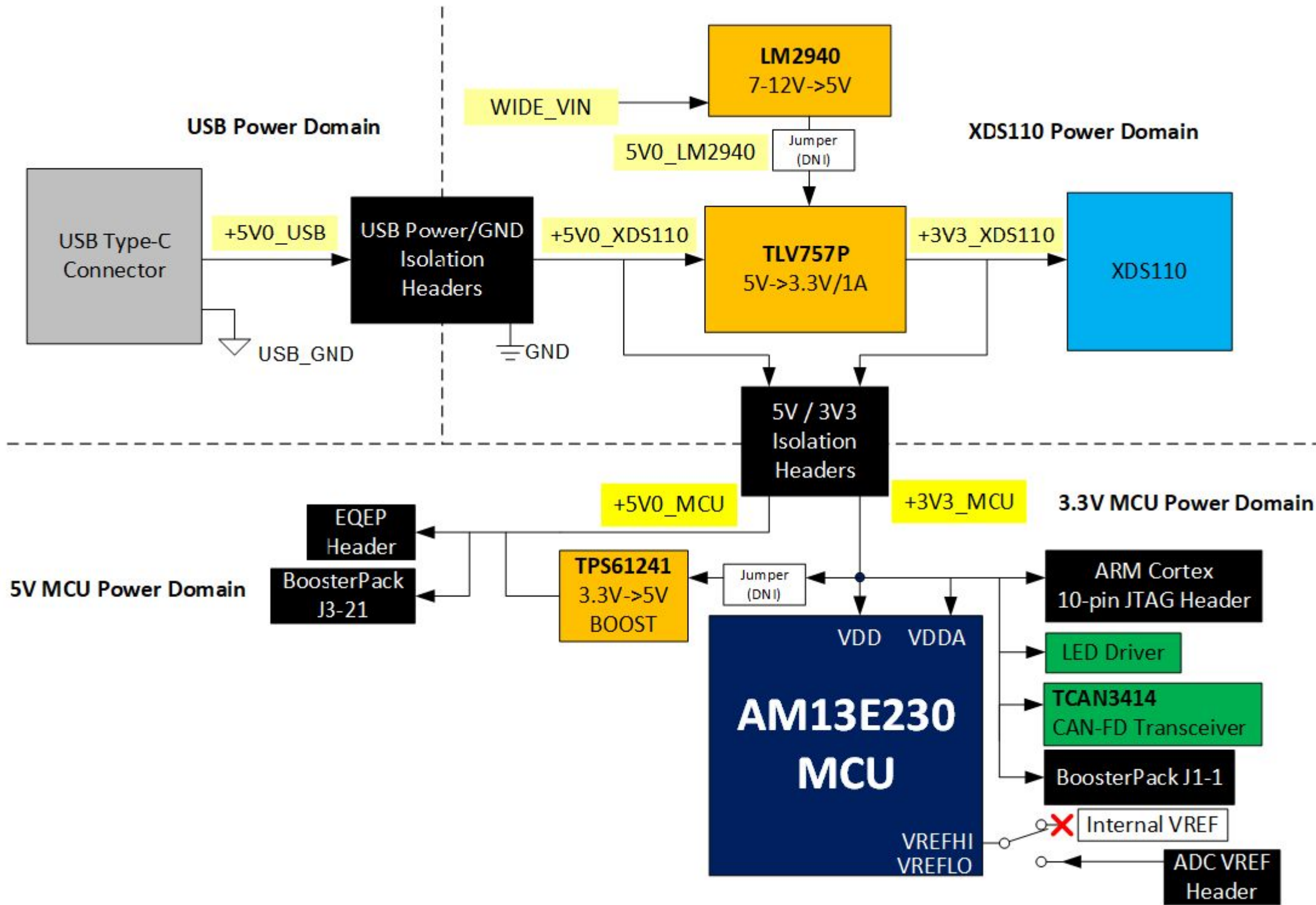
AM13E230 LaunchPad EVM



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Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 9/5/2025
TID #: N/A	Project Title: LP-AM13E230	
Number: MCU178	Rev: E2	Sheet: 1 of 10
SVN Rev:	Assembly Variant: 001	Size: B
Drawn By:	File: MCU178E2_01_BlockDiagram.SchDoc	
Engineer: Brennan Hartigan	Contact: http://www.ti.com/support	

Power Tree

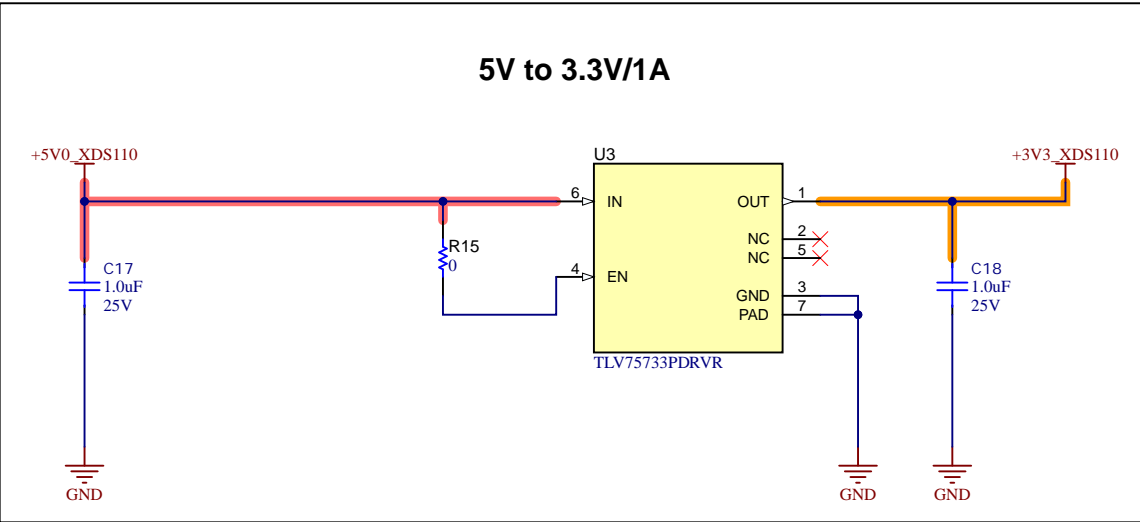


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Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 9/5/2025
TID #: N/A	Project Title: LP-AM13E230	
Number: MCU178	Rev: E2	Sheet Title:
SVN Rev:	Assembly Variant: 001	Sheet: 2 of 10
Drawn By:	File: MCU178E2_02_PowerTree.SchDoc	Size: B
Engineer: Brennan Hartigan	Contact: http://www.ti.com/support	

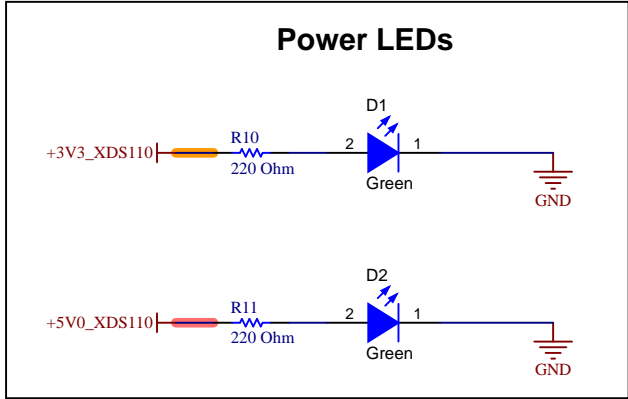
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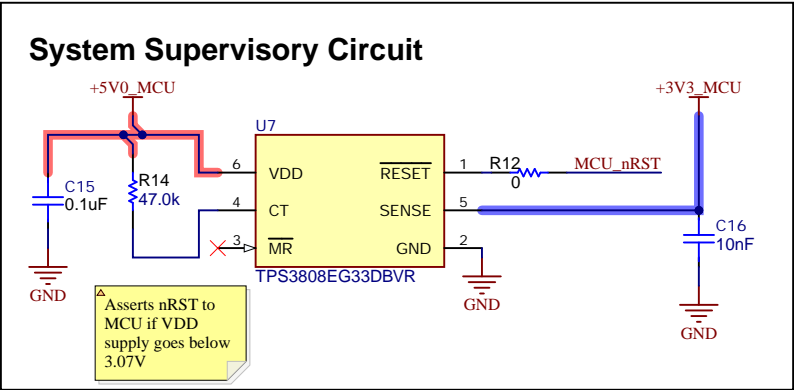
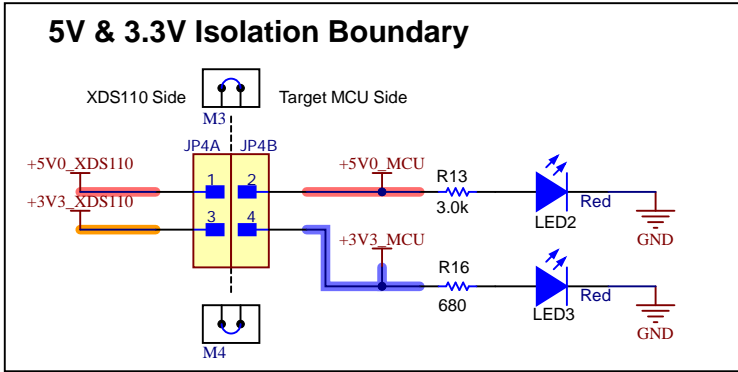


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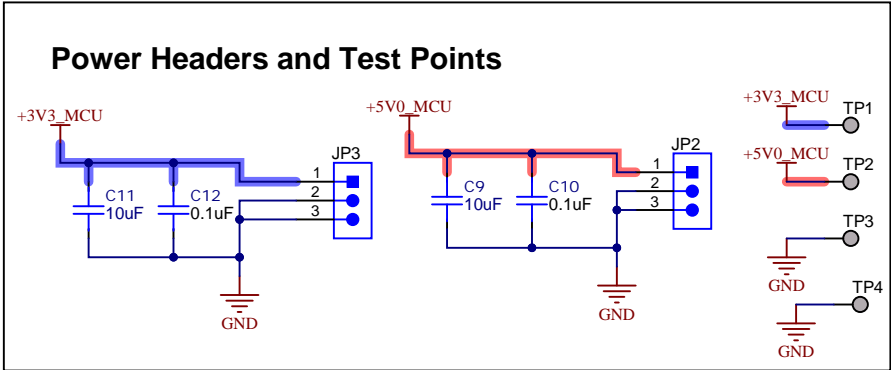
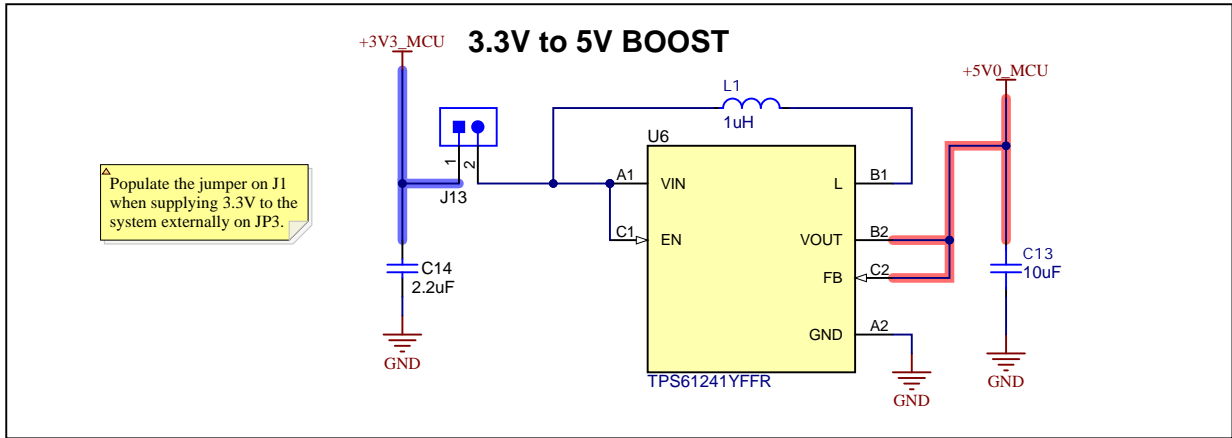
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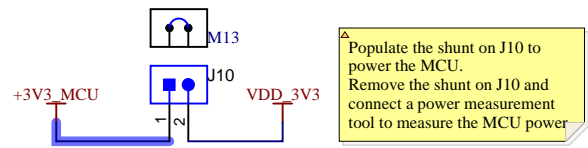
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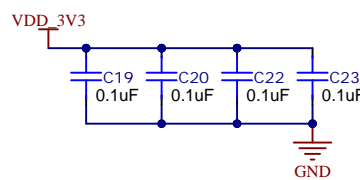
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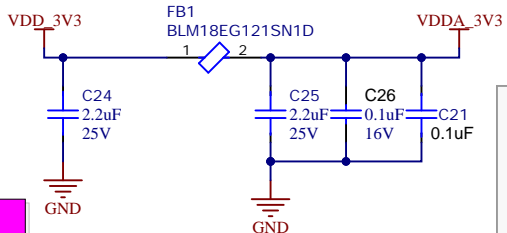
Power Isolation / Measurement Jumper



VDD 3V3 Digital

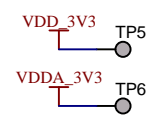


VDDA 3V3 Analog

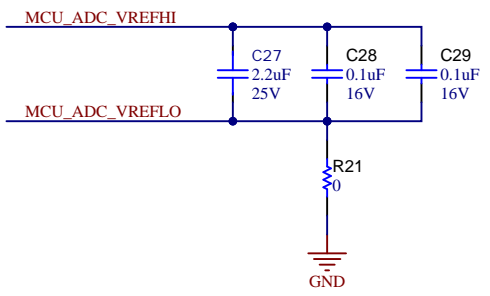


Place decoupling as close as possible to MCU

MCU Supply TPs

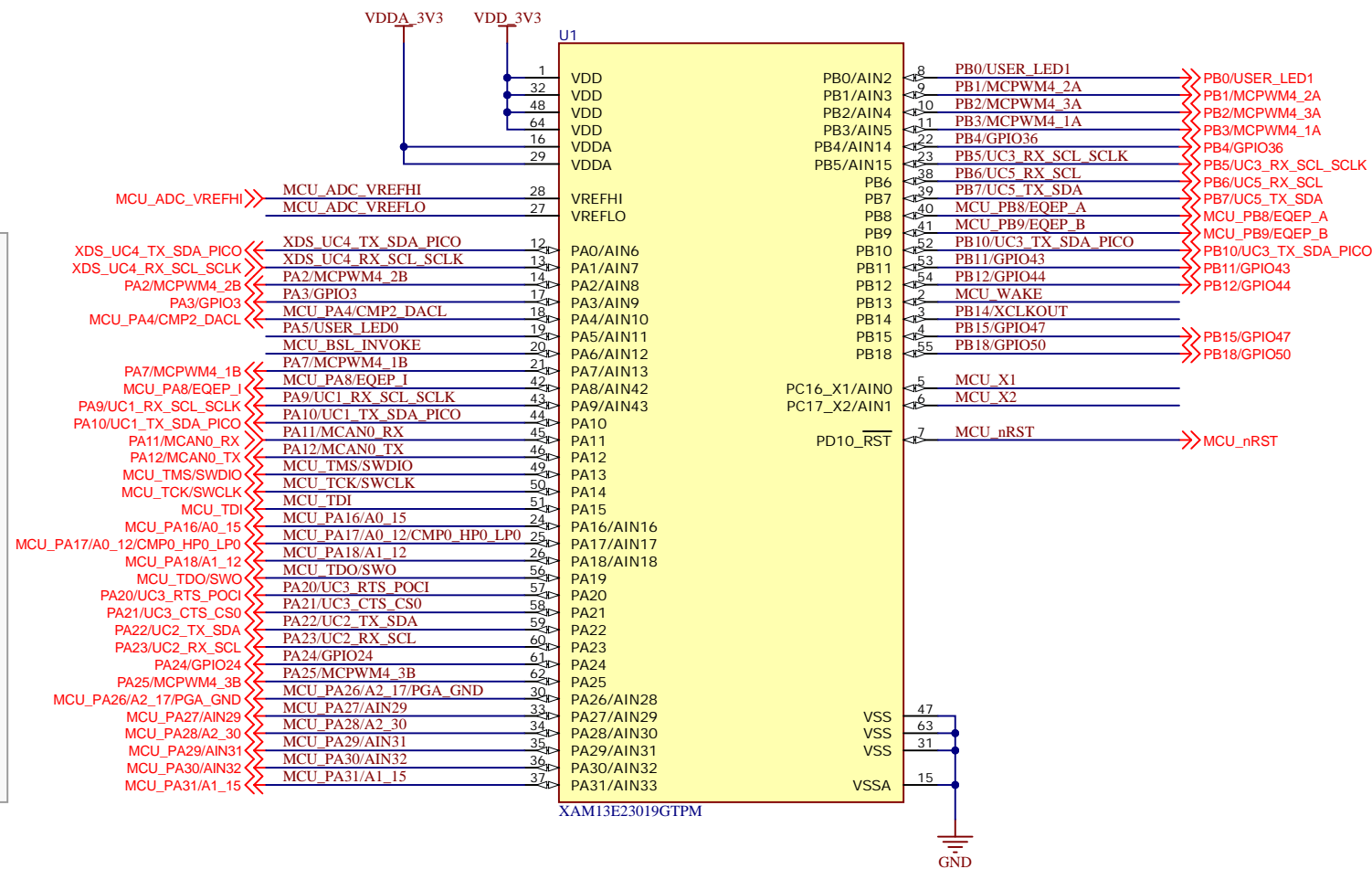


ADC VREF



J12	XDS110 UART RX	
J12	XDS110 UART TX	
J4_37	MCPWM	
J1_5	GPIO	
J3_30	DAC	
J4_39	MCPWM	
J5_3	EQEP	
J1_3	UART RX	
J1_4	UART TX	
J4_31	CAN RX	
J4_32	CAN TX	
J3_23	ADC	
J3_26	ADC/CMP	
J3_24	ADC	
J2_14	SPI POCI	
J2_19	SPI CS	
J1_10	I2C SDA	
J1_9	I2C SCL	
J2_17	GPIO	
J4_35	MCPWM	
J1_2	ADC/PGA GND	
J3_27	ADC/PGA IN	
J3_25	ADC	
J3_29	ADC/PGA IN	
J3_28	ADC/PGA IN	
J1_6	ADC	

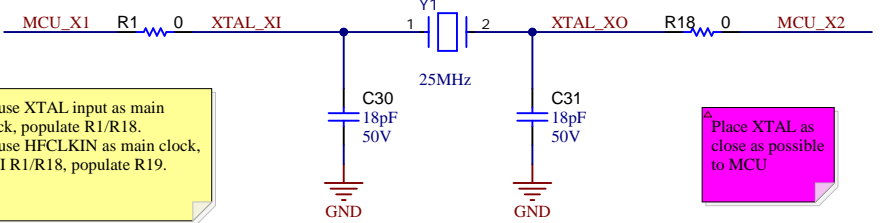
AM13E230 MCU



MCPWM	J4_38
MCPWM	J4_36
MCPWM	J4_40
GPIO	J1_8
SPI CLK	J1_7
LIN RX	J4_33
LIN TX	J4_34
EQEP	J5_1
EQEP	J5_2
SPI PICO	J2_15
GPIO	J2_11
GPIO	J2_12
GPIO	J2_18
GPIO	J2_13
nRST	J2_16

Clocks

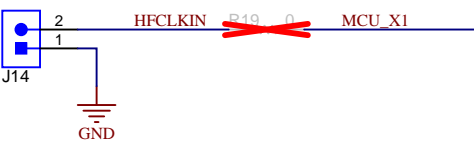
25MHz Crystal (Default)



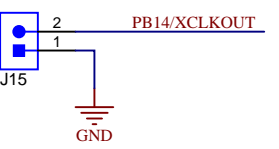
To use XTAL input as main clock, populate R1/R18. To use HFCLKIN as main clock, DNI R1/R18, populate R19.

Place XTAL as close as possible to MCU

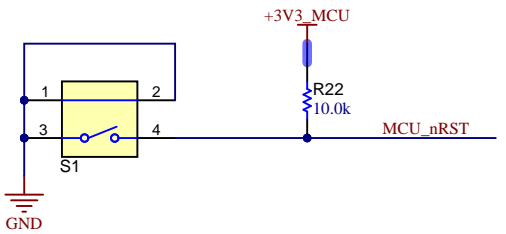
High-Frequency Oscillator Input



External Clock Output



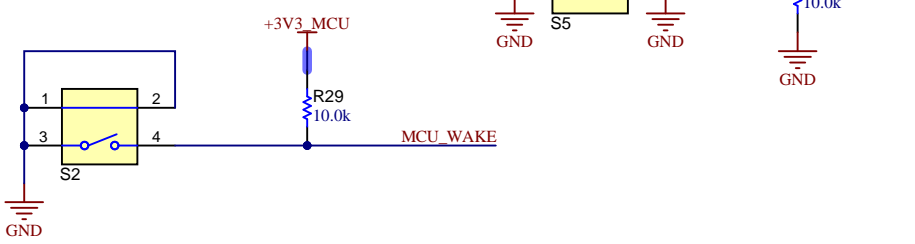
MCU Reset



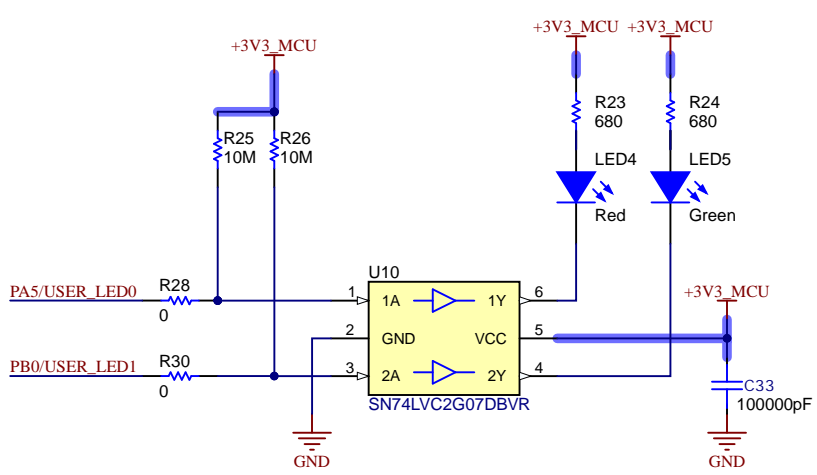
BSL Invoke

Populate J11 to invoke BSL through hardware.

Wake/User Input



User LEDs



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A

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B

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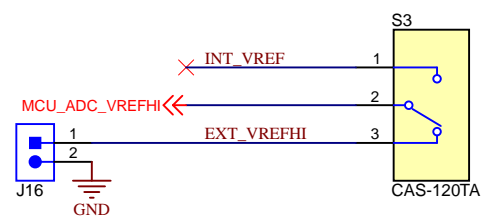
C

C

D

D

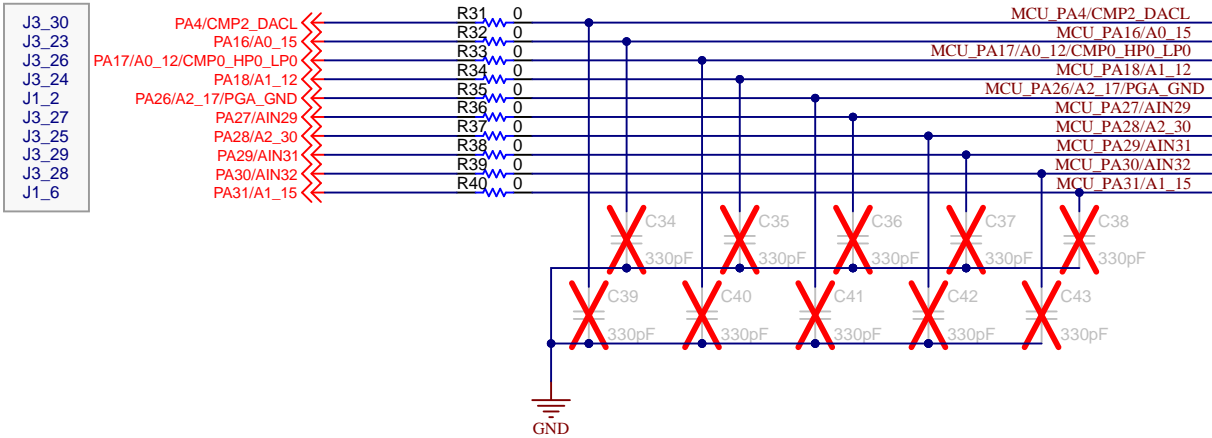
ADC VREF DIP SWITCH



ADC VREF VOLTAGE SELECTION (S3)

SW POSITION	SUPPLY SELECTION
PIN 1-2 DEFAULT	Select internal reference voltage
PIN 2-3	Selects external reference voltage

Analog RC Filters

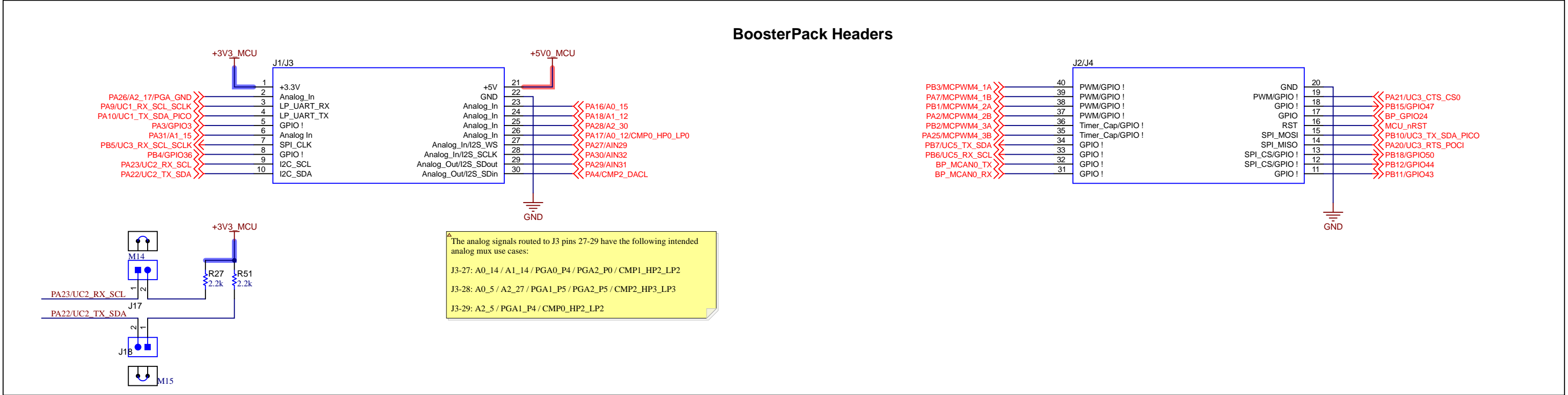


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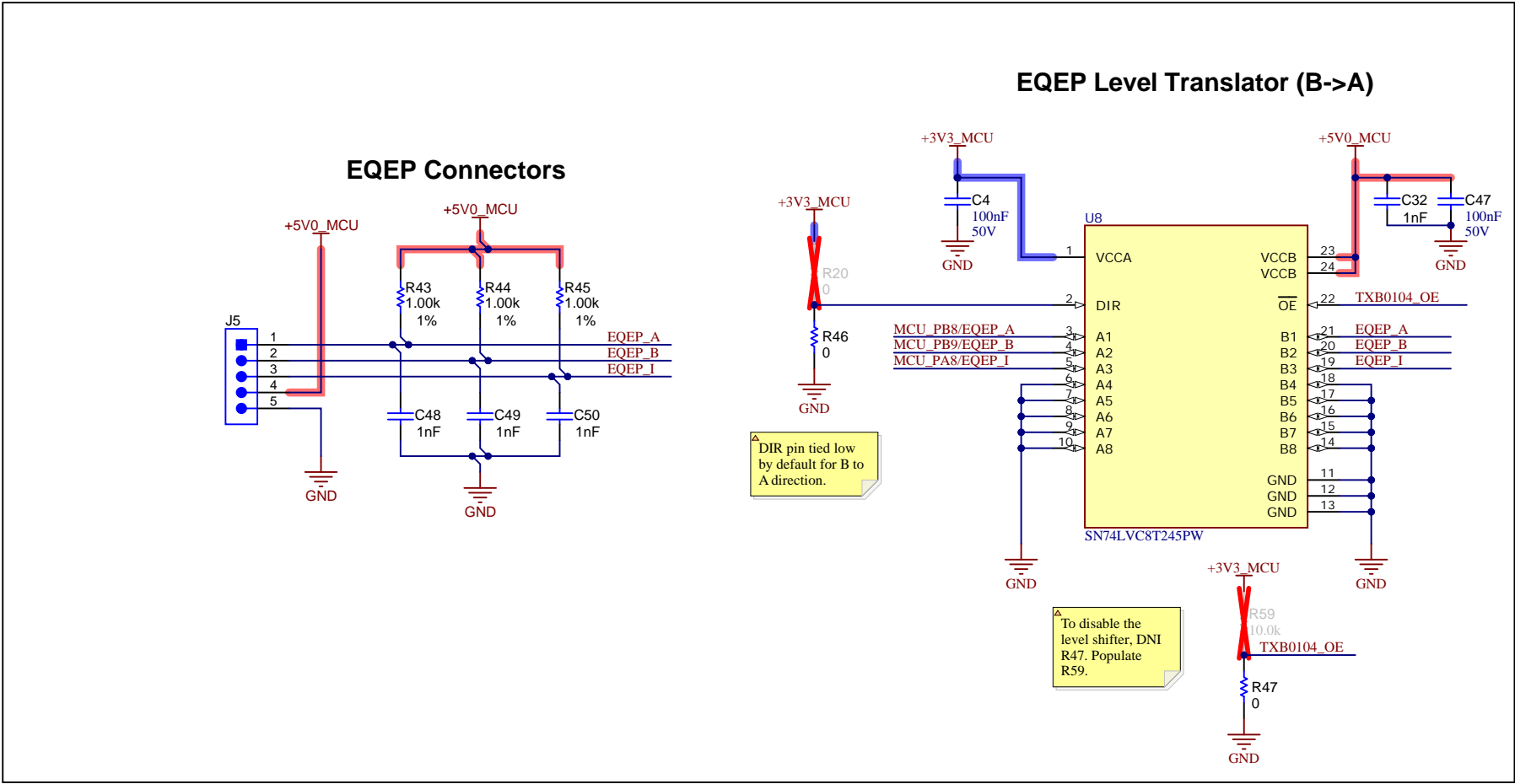


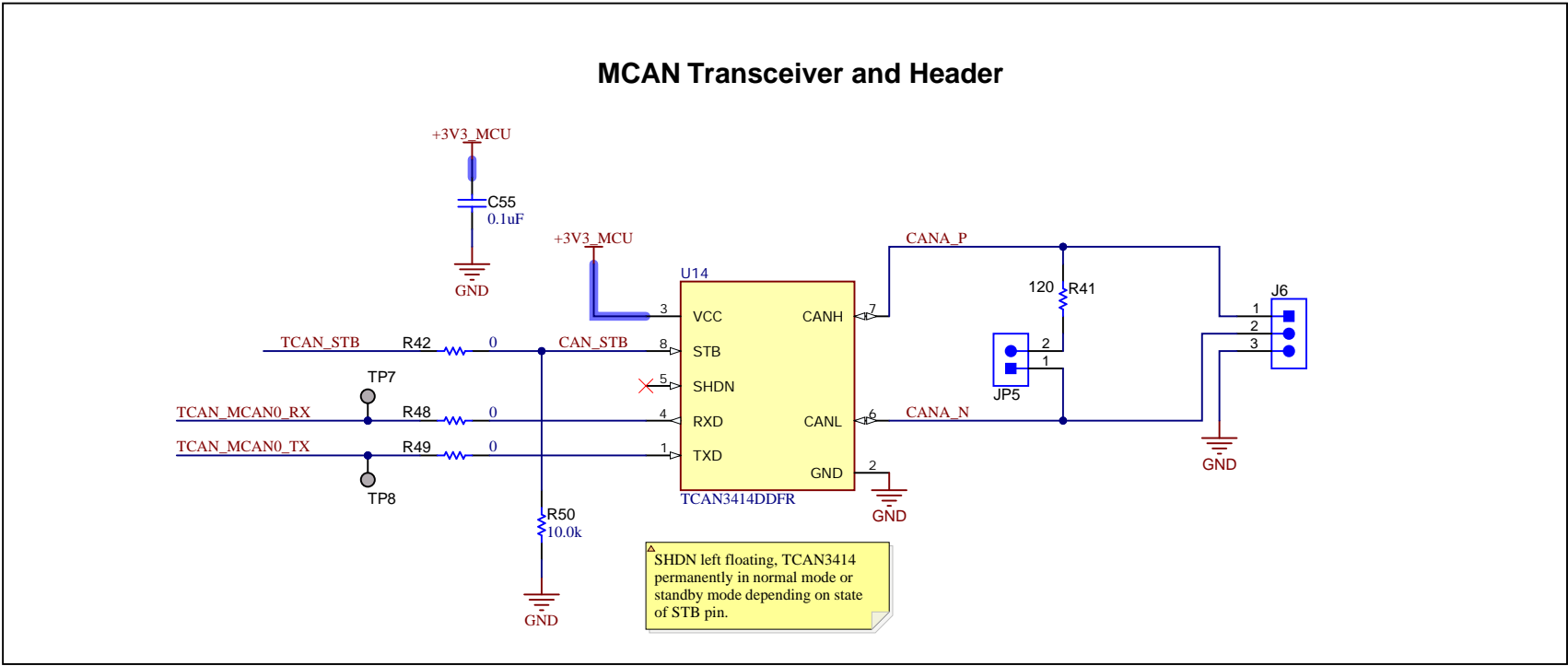
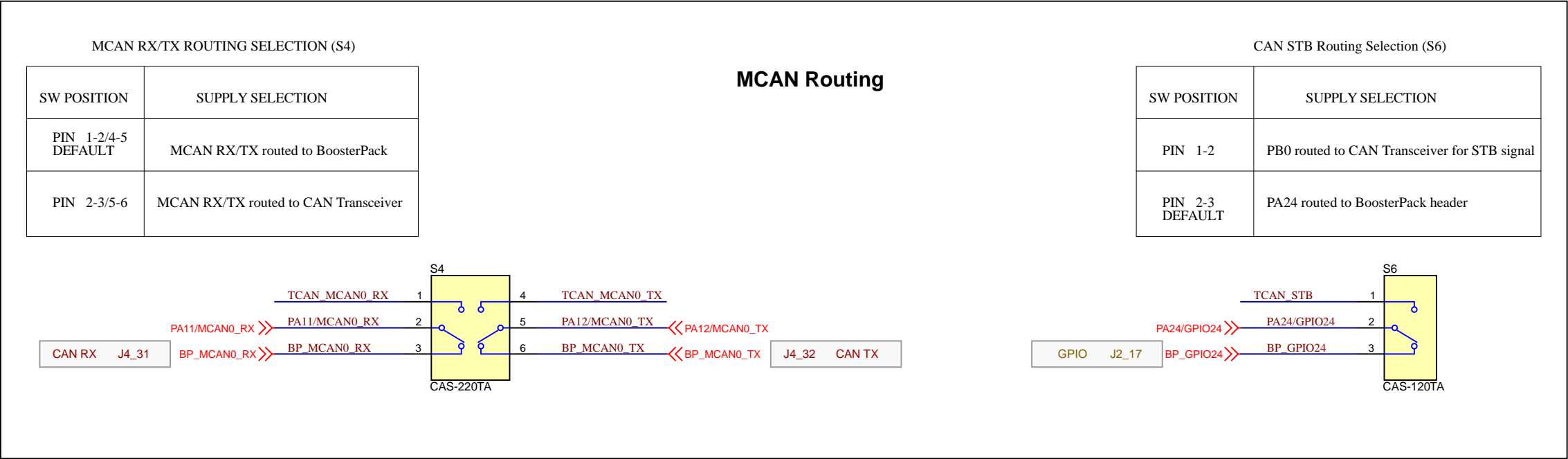
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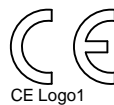
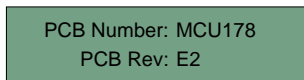
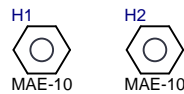
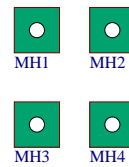
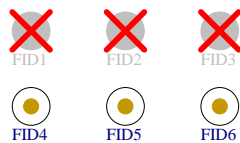
D

C

D







ZZ1

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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TID #: N/A	Project Title: LP-AM13E230		
Number: MCU178	Rev: E2	Sheet Title:	
SVN Rev:	Assembly Variant: 001	Sheet: 10 of 10	
Drawn By:	File: MCU178E2_10_Hardware.SchDoc	Size: B	
Engineer: Brennan Hartigan		Contact: http://www.ti.com/support	